[Document name] Figures

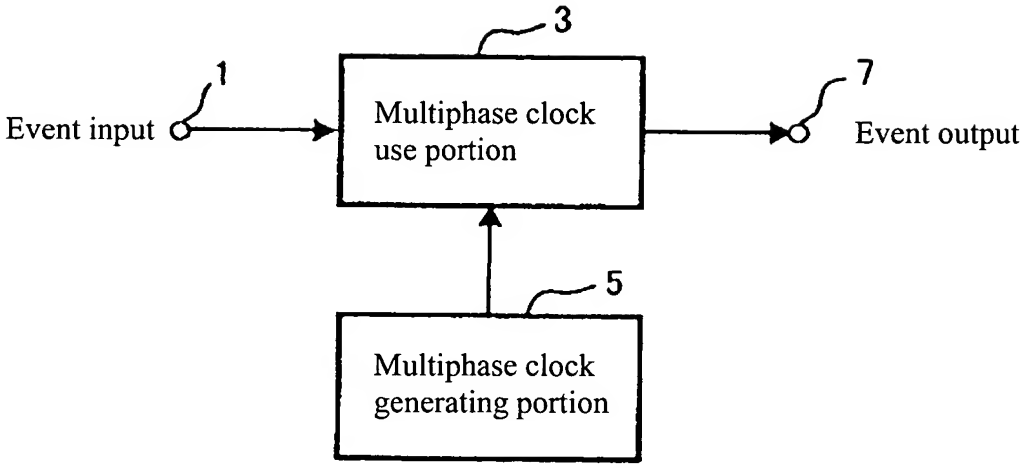

FIG. 1. Event timing adjustment device.

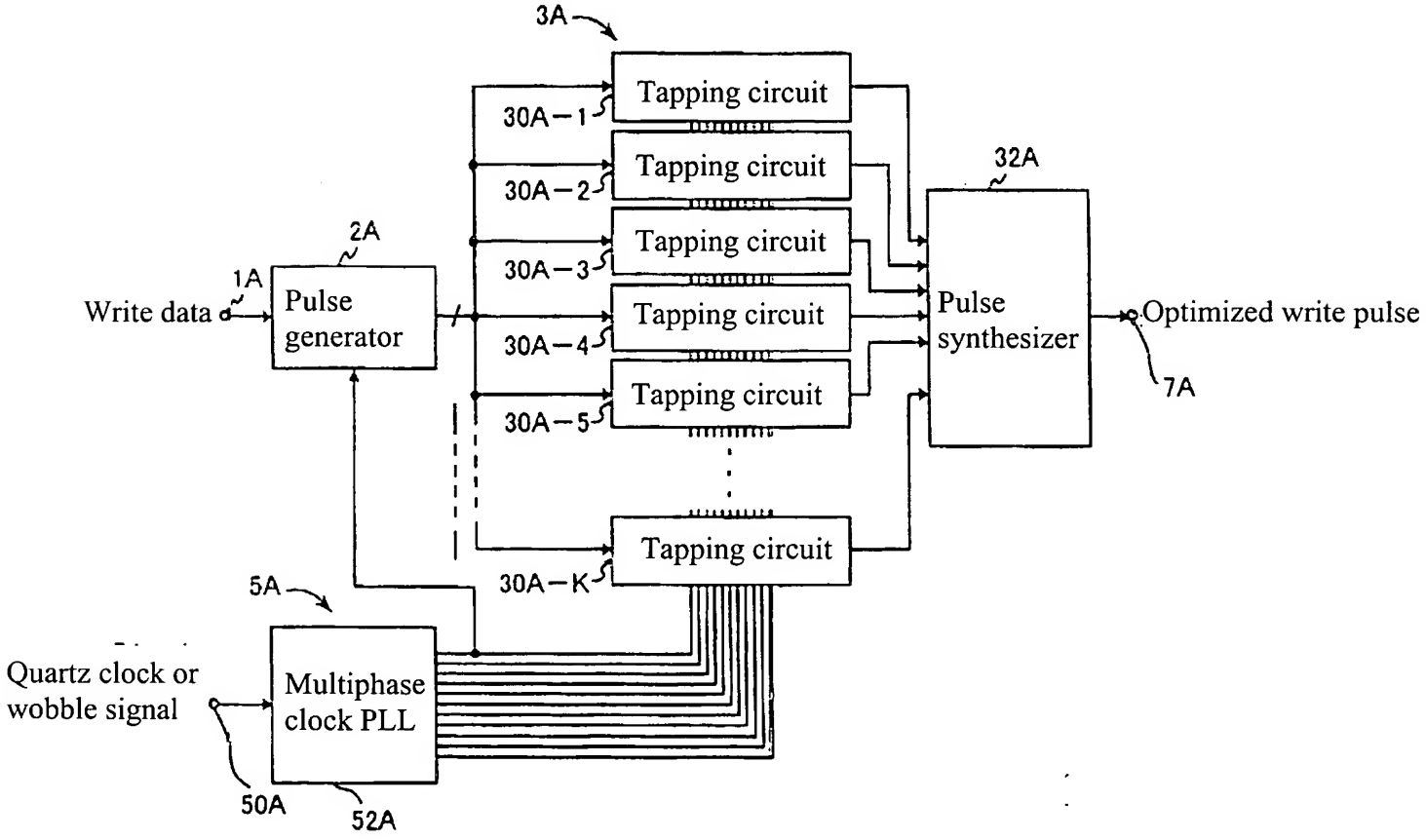

FIG. 2. Pulse width adjusting device A.

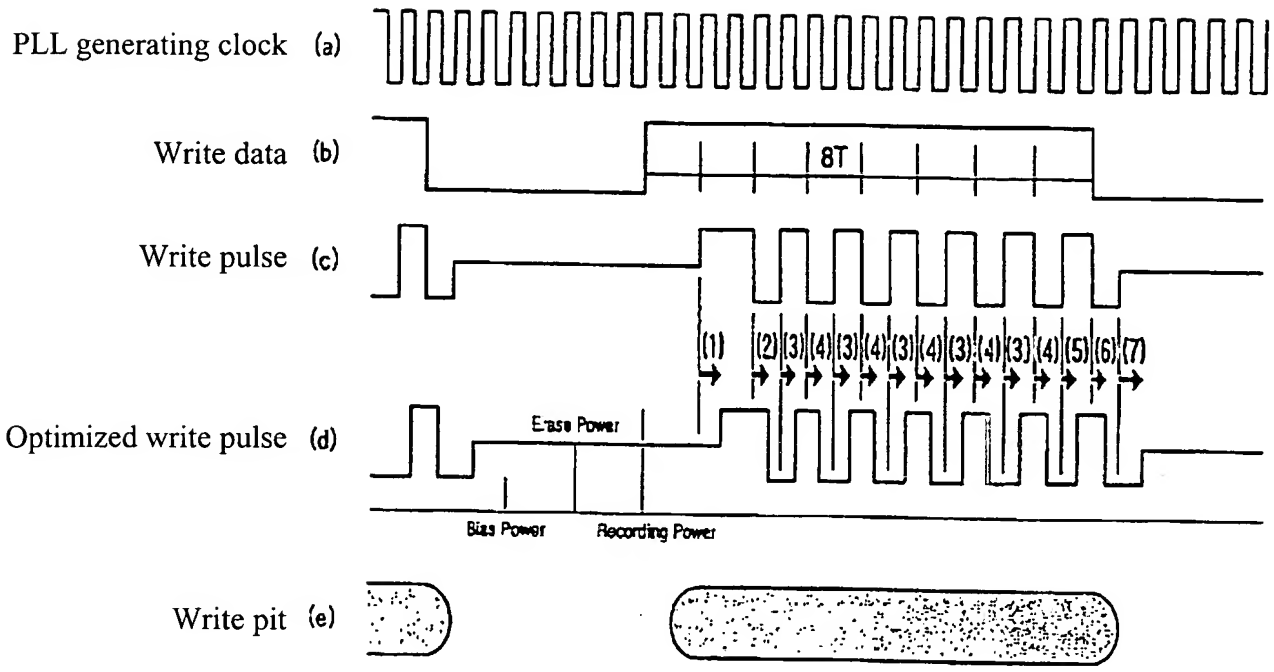
PLL generating clock (a)
Write data (b)
8T
Write pulse (c)
(1) (2) (3) (4) (3) (4) (3) (4) (3) (4) (3) (4) (5) (6) (7)
Optimized write pulse (d)
Erase Power
Bias Power
Recording Power
Write pit (e)

FIG. 3

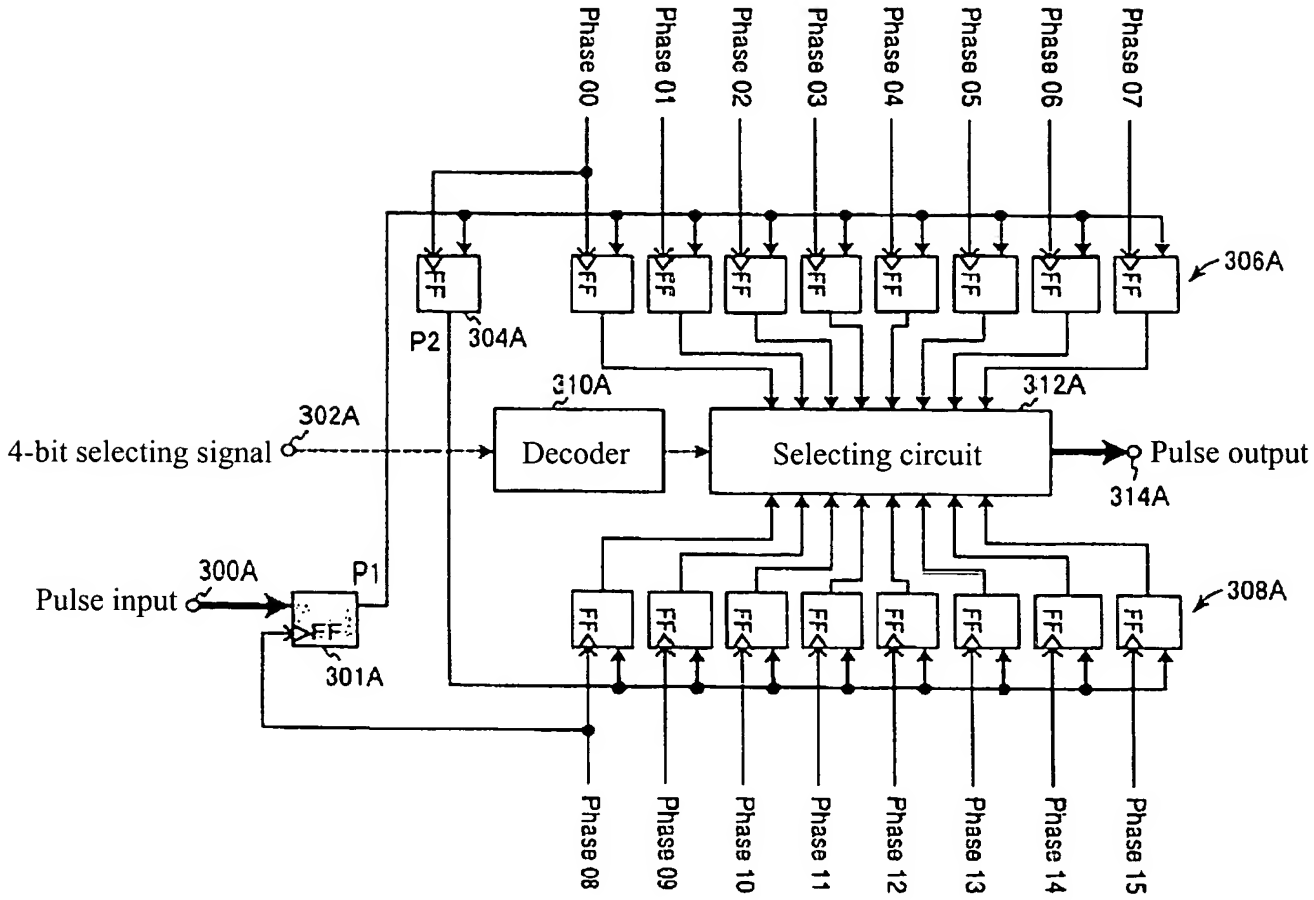

FIG. 4. Delay tapping circuit 30A-k

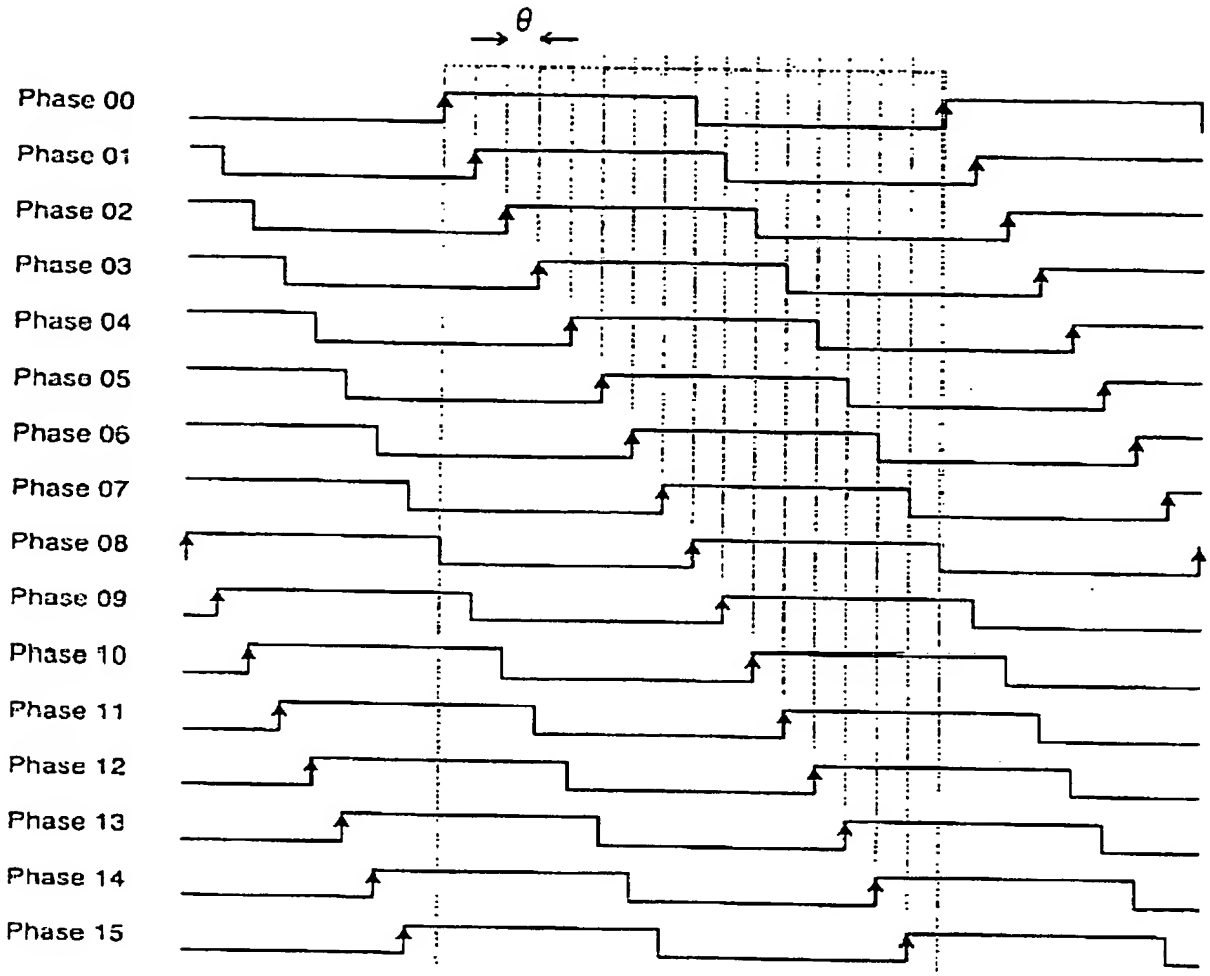
θ
Phase 00
Phase 01
Phase 02
Phase 03
Phase 04
Phase 05
Phase 06
Phase 07
Phase 08
Phase 09
Phase 10
Phase 11
Phase 12
Phase 13
Phase 14
Phase 15

FIG. 5

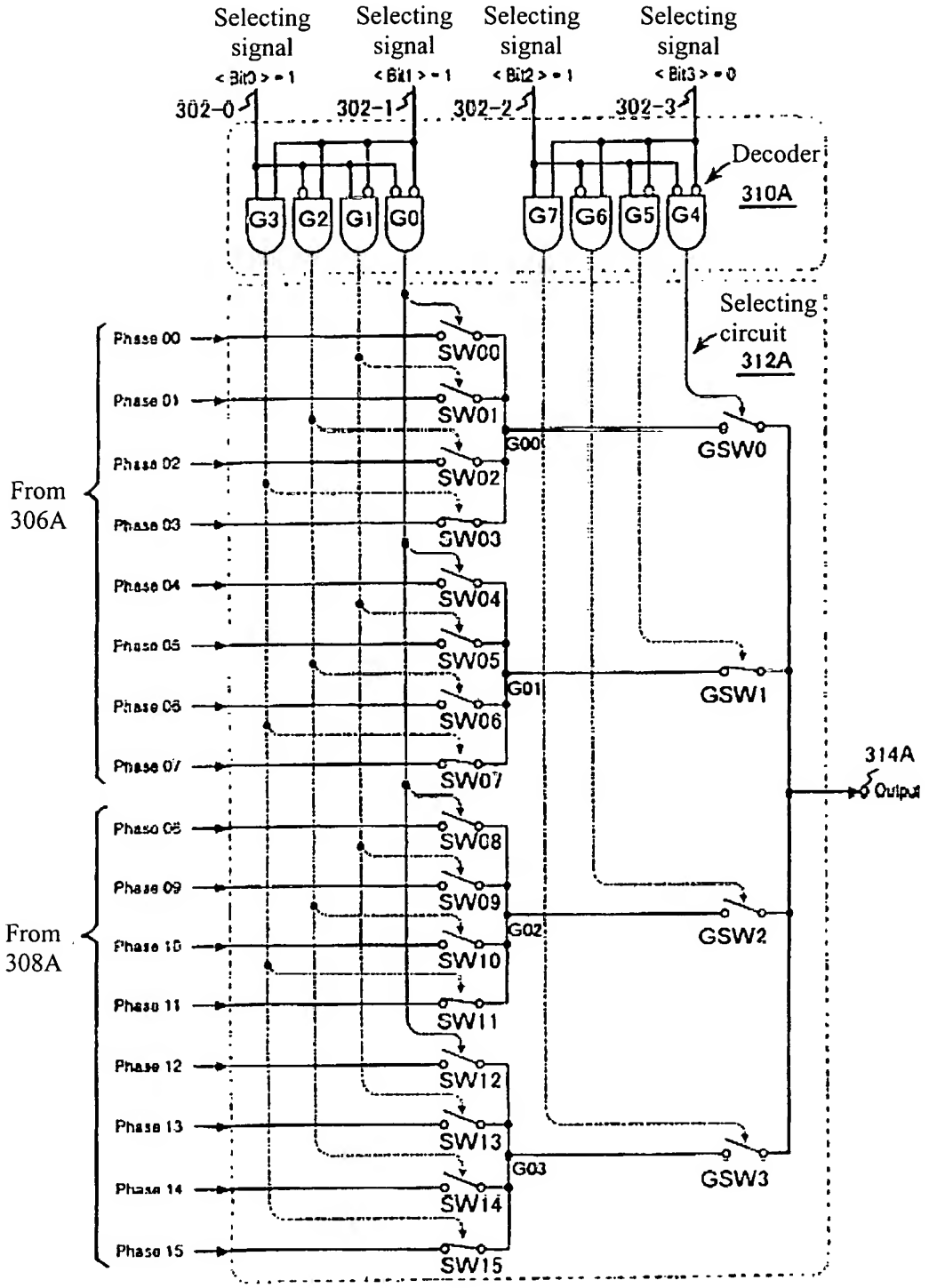
Selecting signal
< Bit0 > = 1
Selecting signal
< Bit1 > = 1
Selecting signal
< Bit2 > = 1
Selecting signal
< Bit3 > = 0
302-0
302-1
302-2
302-3
Decoder
310A
G3
G2
G1
G0
G7
G6
G5
G4
Selecting circuit
312A
From 306A
From 308A
Phase 00
Phase 01
Phase 02
Phase 03
Phase 04
Phase 05
Phase 06
Phase 07
Phase 08
Phase 09
Phase 10
Phase 11
Phase 12
Phase 13
Phase 14
Phase 15
SW00
SW01
SW02
SW03
SW04
SW05
SW06
SW07
SW08
SW09
SW10
SW11
SW12
SW13
SW14
SW15
G00
G01
G02
G03
GSW0
GSW1
GSW2
GSW3
314A
Output

FIG. 6

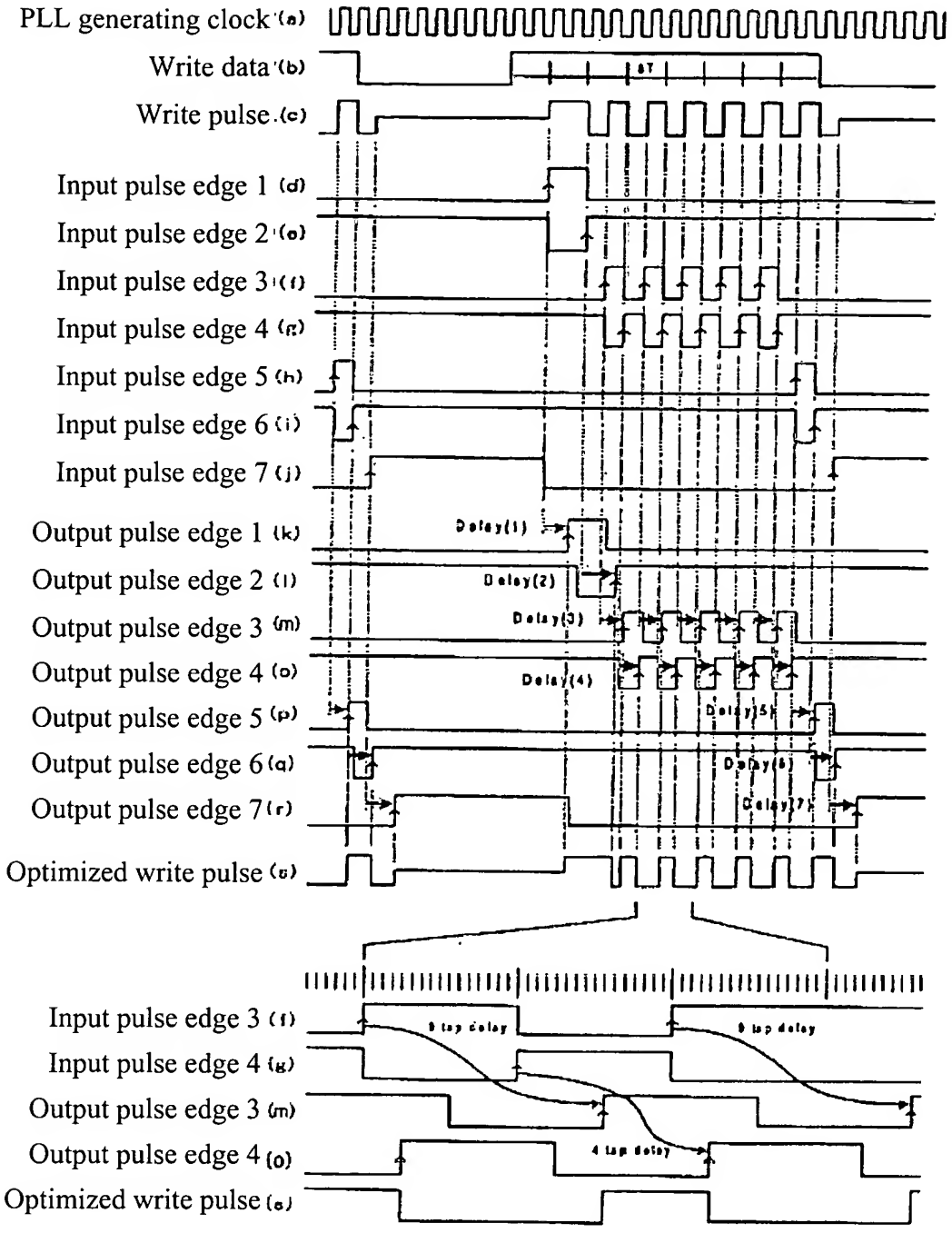
PLL generating clock (a)
Write data (b)
Write pulse (c)
Input pulse edge 1 (d)
Input pulse edge 2 (e)
Input pulse edge 3 (f)
Input pulse edge 4 (g)
Input pulse edge 5 (h)
Input pulse edge 6 (i)
Input pulse edge 7 (j)
Output pulse edge 1 (k)
Output pulse edge 2 (l)
Output pulse edge 3 (m)
Output pulse edge 4 (n)
Output pulse edge 5 (p)
Output pulse edge 6 (q)
Output pulse edge 7 (r)
Optimized write pulse (s)
Delay(1)
Delay(2)
Delay(3)
Delay(4)
Delay(5)
Delay(6)
Delay(7)
Input pulse edge 3 (f)
Input pulse edge 4 (g)
Output pulse edge 3 (m)
Output pulse edge 4 (o)
Optimized write pulse (s)
8 tap delay
8 tap delay
4 tap delay

FIG. 7

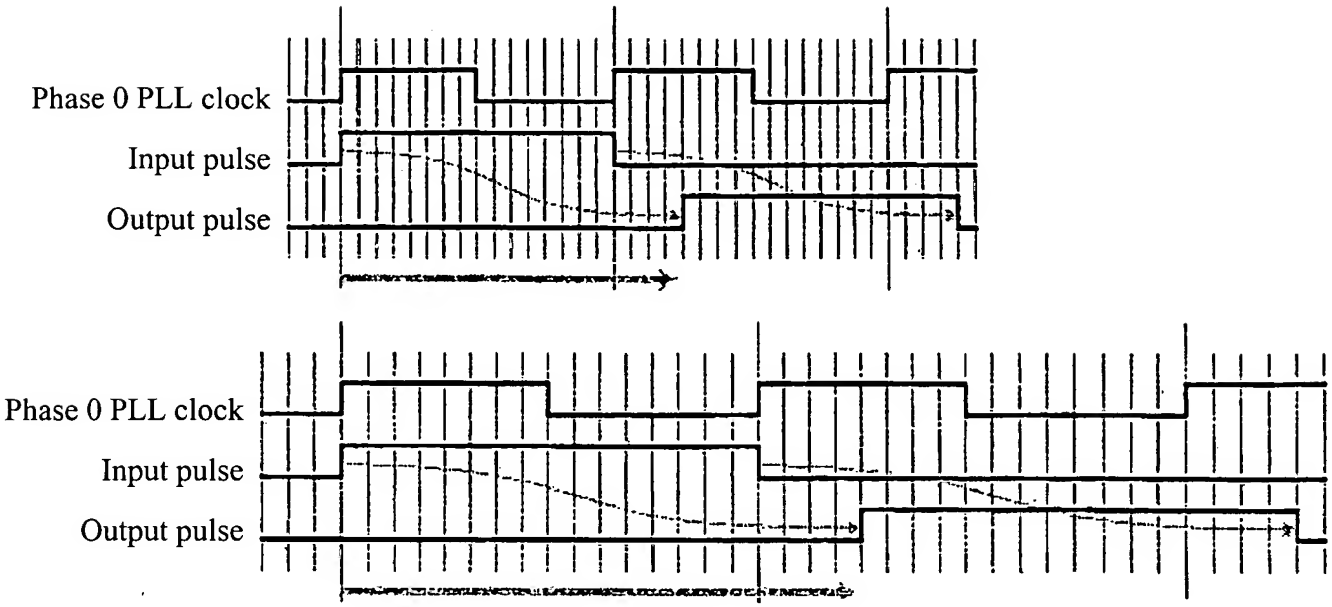
Phase 0 PLL clock
Input pulse
Output pulse
Phase 0 PLL clock
Input pulse
Output pulse

FIG. 8

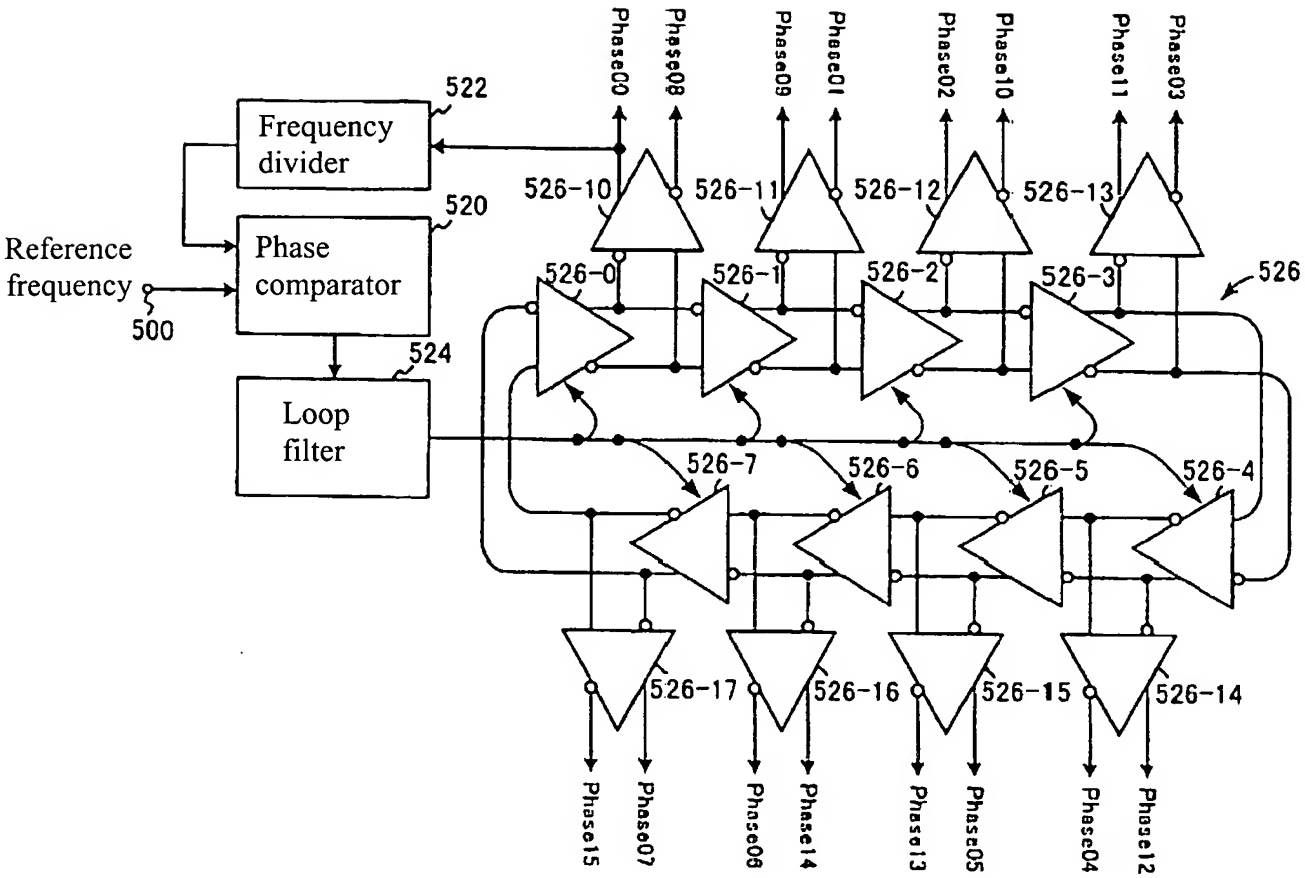

FIG. 9. Multiphase clock PLL circuit 52A.

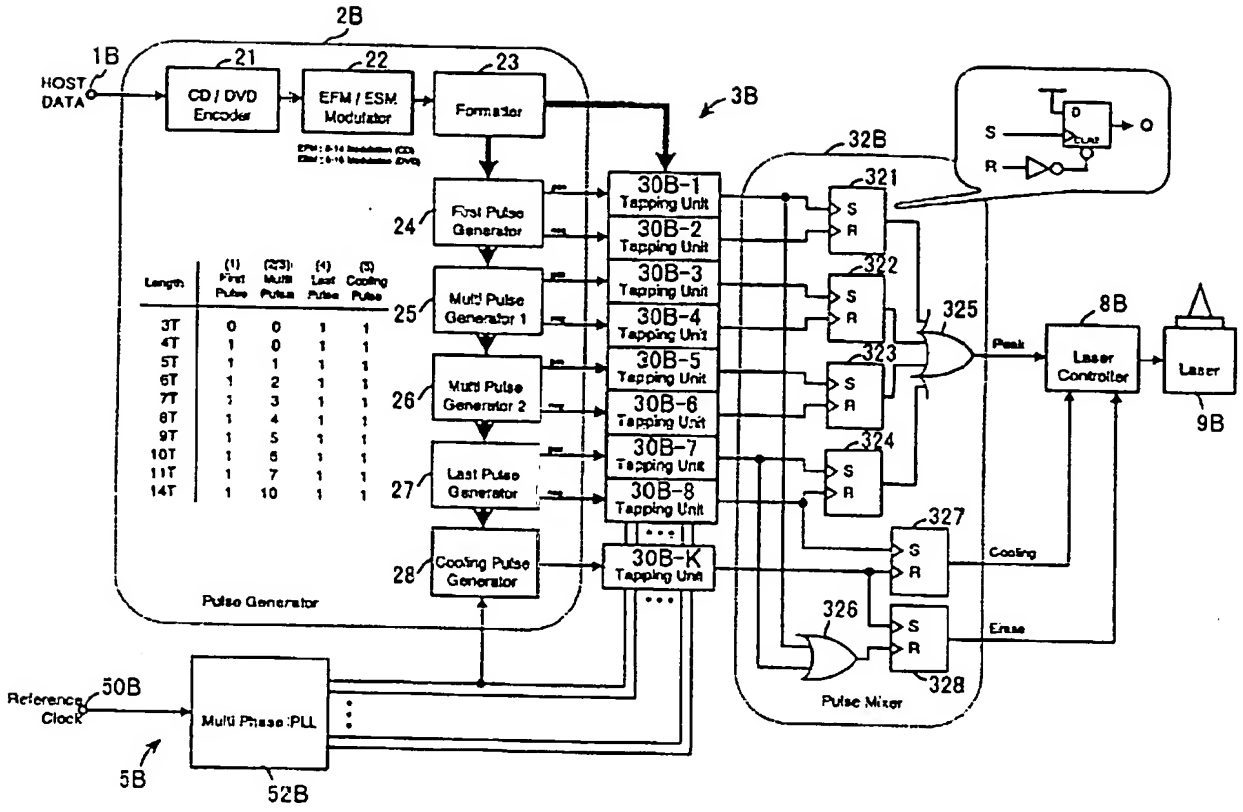

FIG. 10. Optical disk recorder B

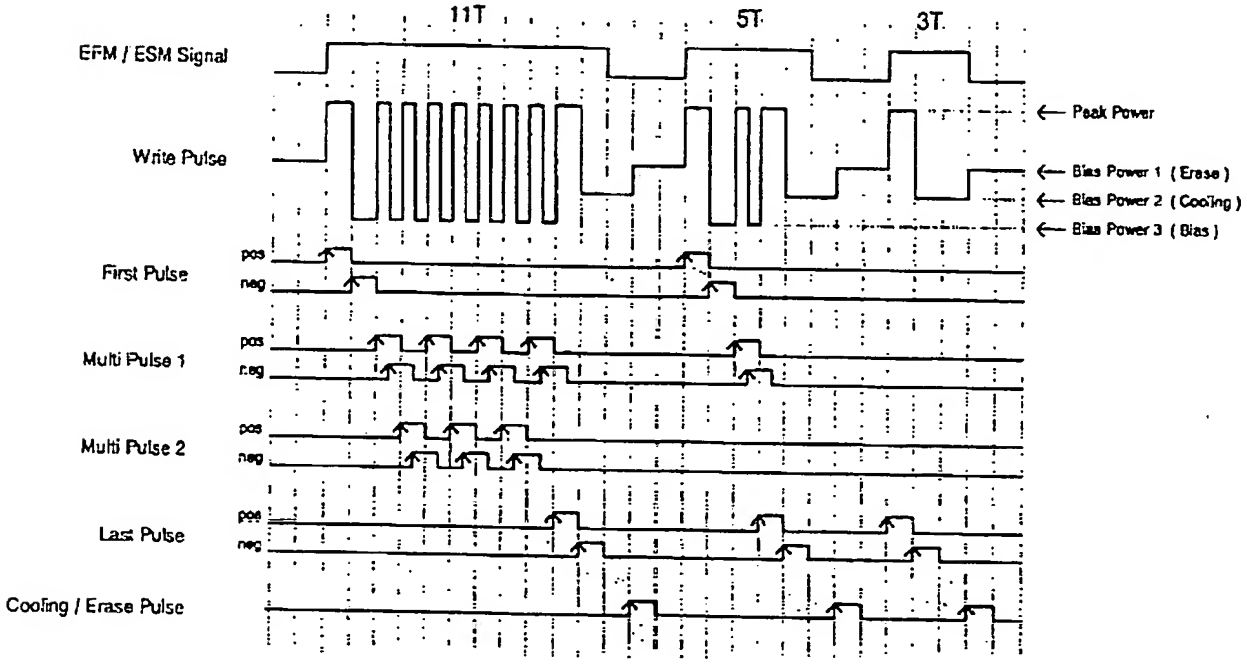

FIG. 11

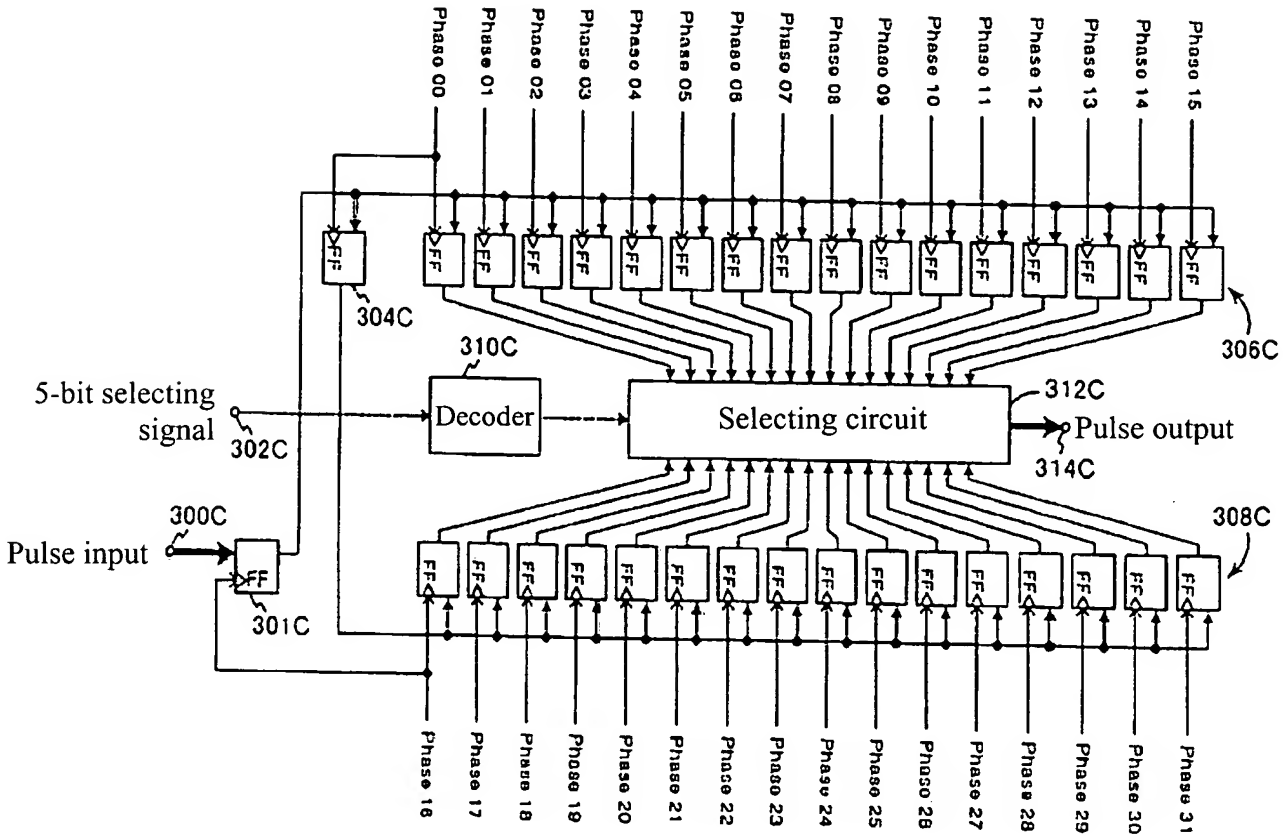

FIG. 12. Delay tapping circuit 30C

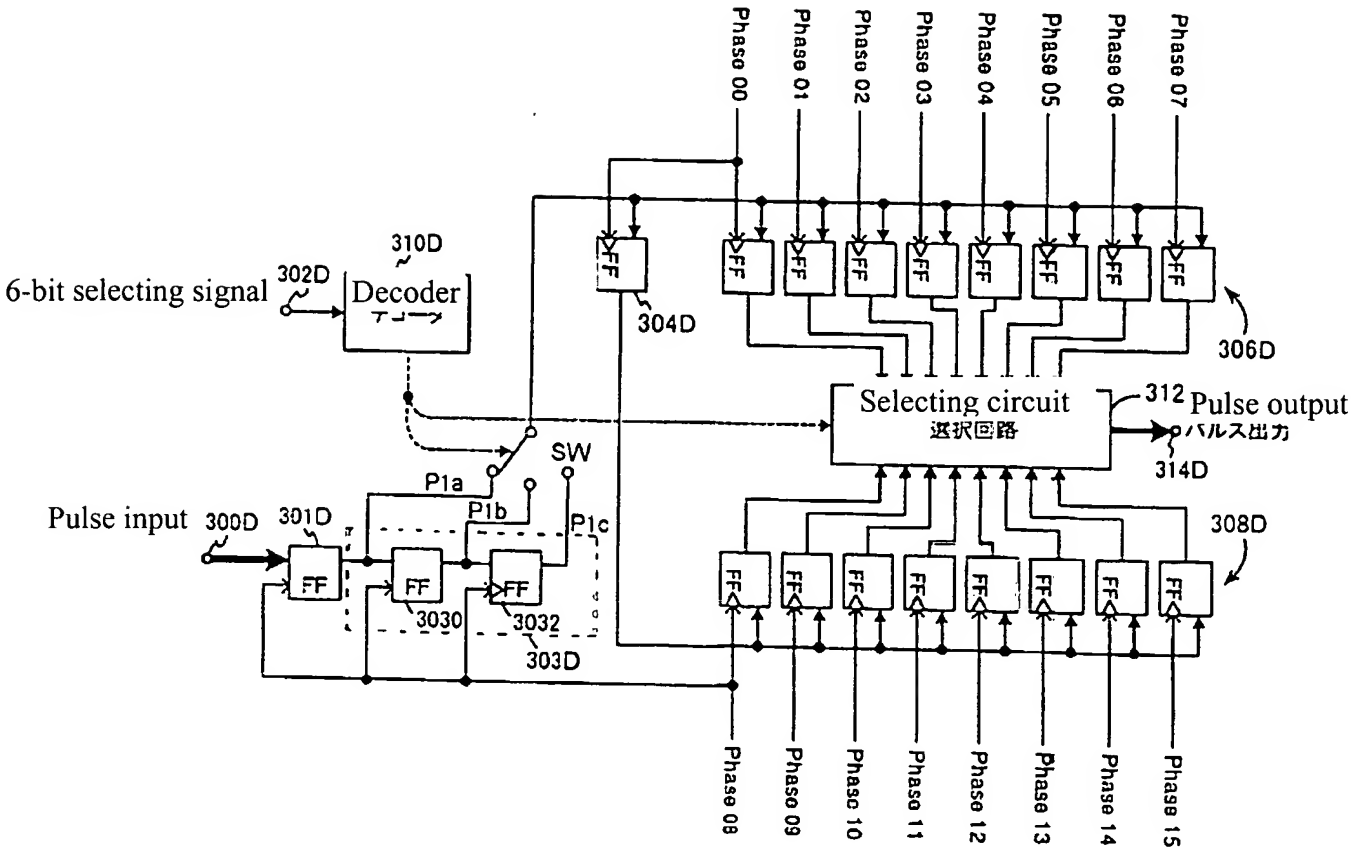

FIG. 13. Delay tapping circuit 30D

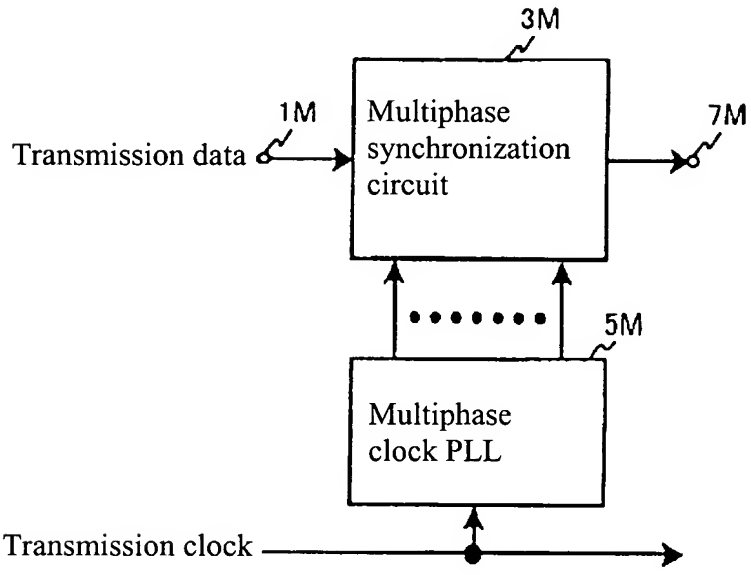

FIG. 14. Synchronization device M.

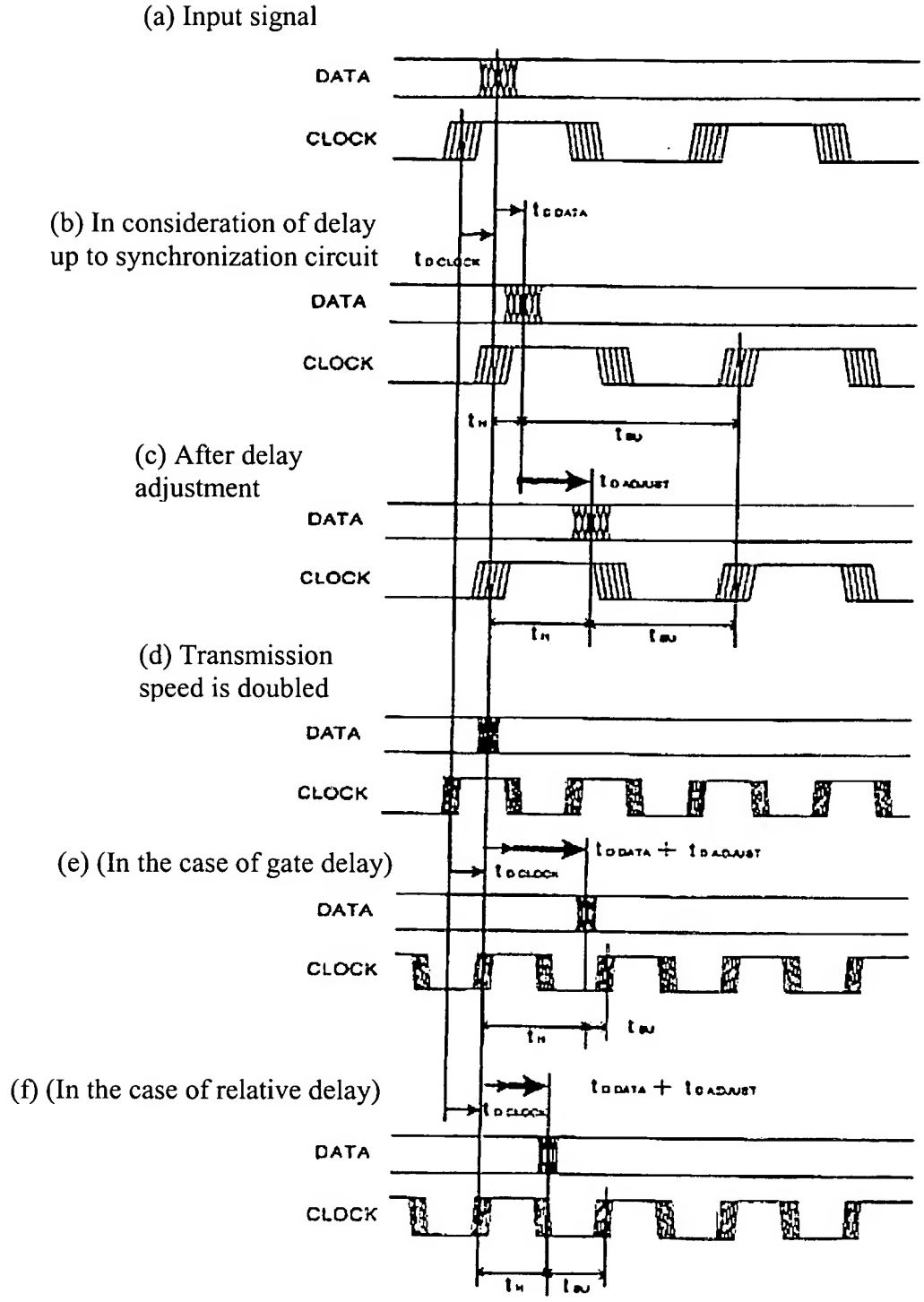
(a) Input signal
DATA
CLOCK
(b) In consideration of delay up to synchronization circuit
DATA
CLOCK
(c) After delay adjustment
DATA
CLOCK
(d) Transmission speed is doubled
DATA
CLOCK
(e) (In the case of gate delay)
DATA
CLOCK
(f) (In the case of relative delay)
DATA
CLOCK

FIG. 15

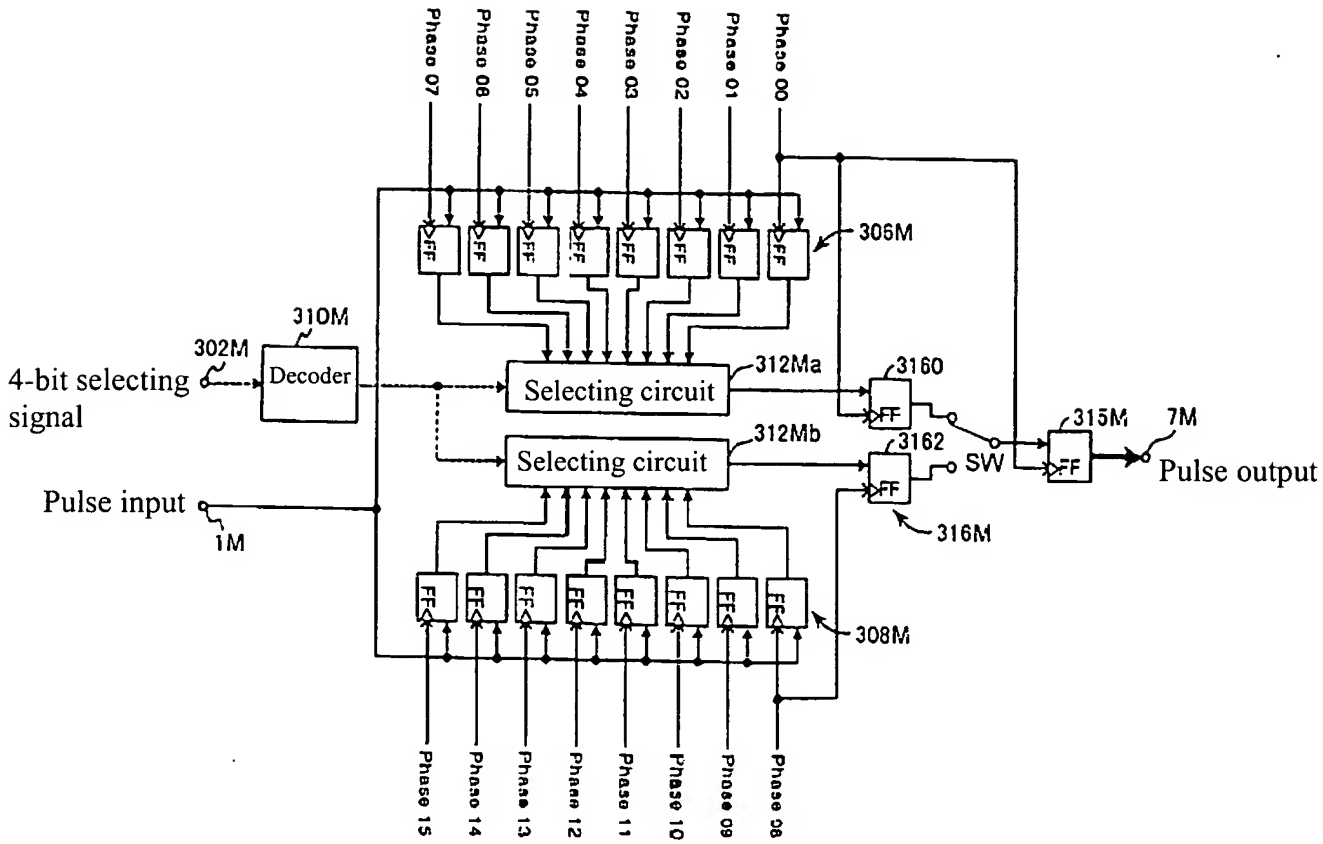

FIG. 16. Multiphase synchronization circuit 3M

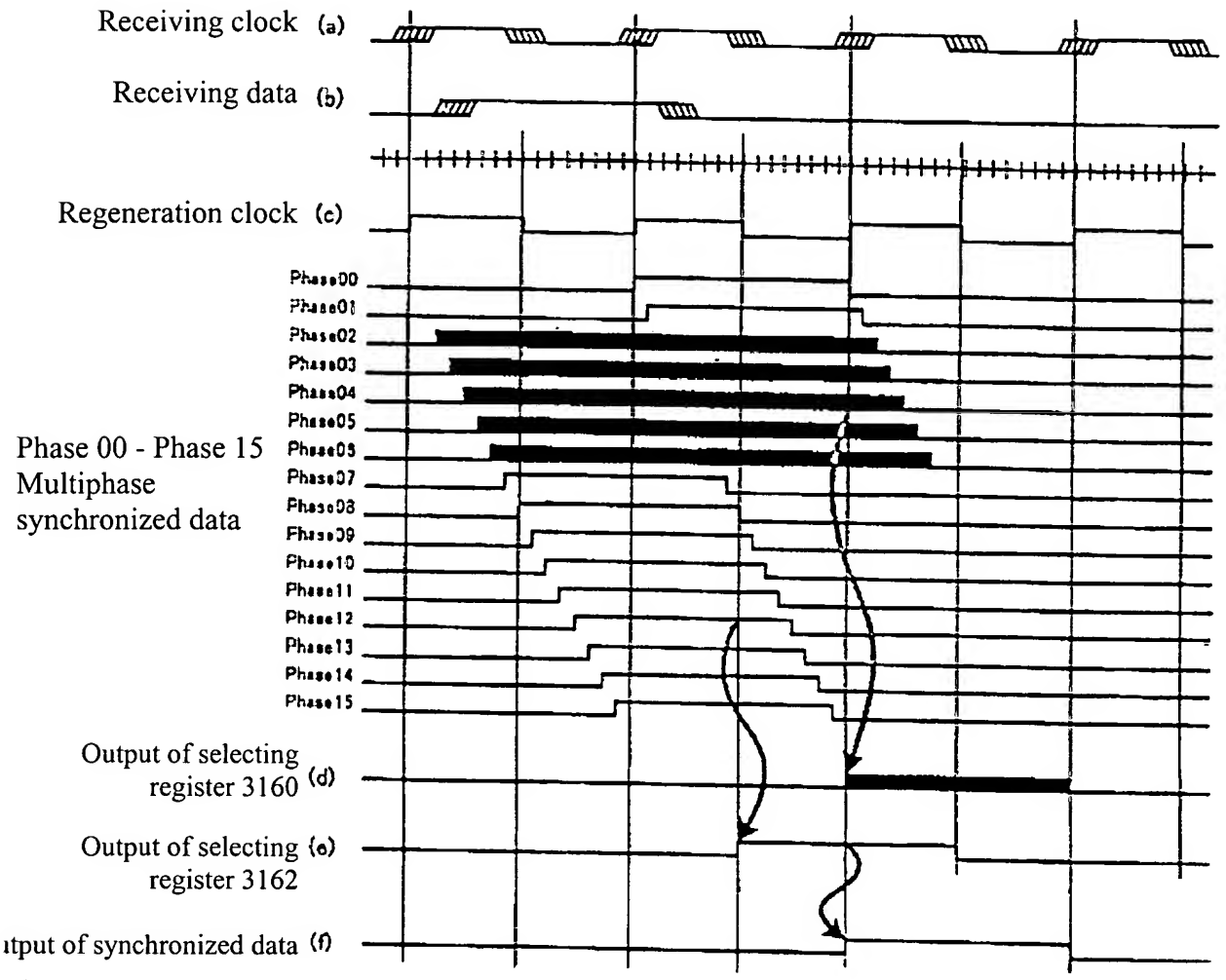
Receiving clock (a)
Receiving data (b)
Regeneration clock (c)
Phase 00 - Phase 15
Multiphase
synchronized data
Output of selecting
register 3160 (d)
Output of selecting (e)
register 3162
itput of synchronized data (f)

FIG. 17